(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
26 April 2007 (26.04.2007)

PCT

(10) International Publication Number
WO 2007/046773 A1

(51) International Patent Classification:
H01L 27/082 (2006.01) *H01L 29/737* (2006.01)
H01L 21/02 (2006.01)

(21) International Application Number:
PCT/SG2006/000255

(22) International Filing Date:
1 September 2006 (01.09.2006)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
200506897-8 19 October 2005 (19.10.2005) SG

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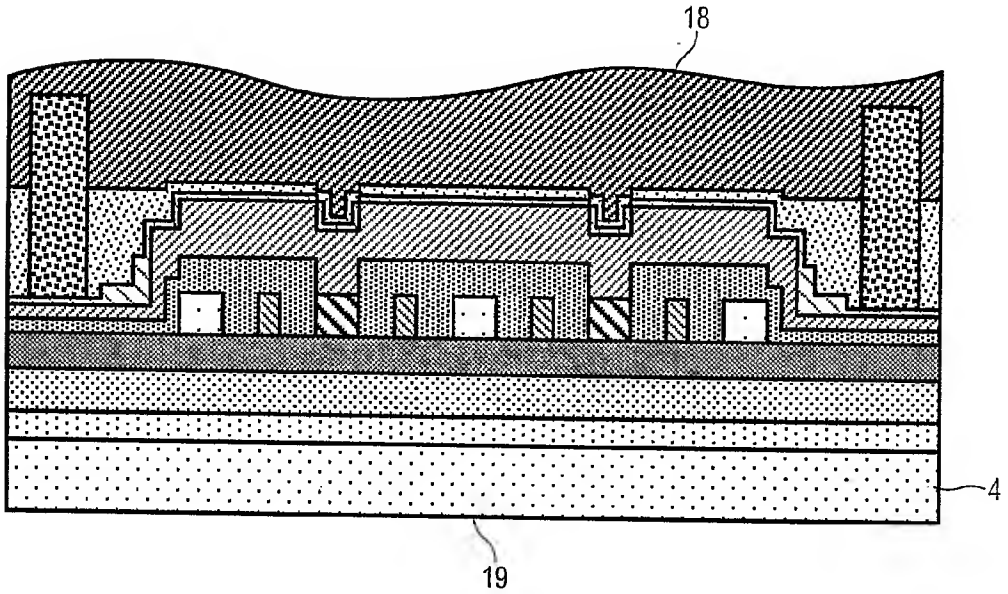
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LV, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Declaration under Rule 4.17:
— *of inventorship (Rule 4.17(iv))*

[Continued on next page]

(54) **Title:** FABRICATION OF TRANSISTORS



(57) **Abstract:** A method for fabricating transistors such as high electron mobility transistors, each transistor comprising a plurality of epitaxial layers on a common substrate, method comprising: (a) forming a plurality of source contacts on a first surface of the plurality of epitaxial layers; (b) forming at least one drain contact on the first surface; (c) forming at least one gate contact on the first surface; (d) forming at least one insulating layer over and between the gate contacts, source contacts and the drain contacts; (e) forming a conductive layer over at least a part of the at least one insulating layer for connecting the source contacts; and (f) forming at least one heat sink layer over the conductive layer.

WO 2007/046773 A1

Published:
— *with international search report*

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.

Fabrication of Transistors

Field of the Invention

This invention relates to the fabrication of transistors and refers particularly, though not exclusively, to the fabrication of gallium nitride high electron mobility transistors ("HEMT") and to transistors so fabricated.

Background of the Invention

HEMT devices have been proposed for a few years. They are capable of high power with over 100W/chip being possible; high frequency – 1 to 40GHz being possible; and can operate at temperatures of over 600°C. This generates a lot of heat so heat dissipation becomes important as not all devices can withstand such temperatures, and the HEMT device may be used with many other devices.

Summary of the Invention

In accordance with a first preferred aspect there is provided a method for fabricating transistors, each transistor comprising a plurality of epitaxial layers on a substrate, method comprising:

forming a plurality of source contacts on a first surface of the plurality of epitaxial layers;

forming at least one drain contact on the first surface;

forming at least one gate contact on the first surface;

forming at least one insulating layer over and between the gate contact, source contacts and drain contact to insulate the gate contact, source contacts and the drain contact;

forming a conductive layer over and through at least a part of the at least one insulating layer for connecting the source contacts; and

forming at least one heat sink layer over the conductive layer.

According to a second preferred aspect there is provided an apparatus comprising transistors, each transistor comprising:

a plurality of epitaxial layers having a first surface;

a plurality source contacts, at least one drain contact, and at least one gate contact, all on the first surface;

at least one insulating layer over and between the gate contact, source contacts and drain contact for insulating the gate contact, source contacts and the drain contact;

a conductive layer over and through at least a part of the at least one insulating layer for connecting the source contacts; and

at least one heat sink layer over the conductive layer.

The transistors may be high electron mobility transistors. The plurality of epitaxial layers may comprise a layer of gallium nitride, a layer of aluminium gallium nitride, a layer of n+ aluminium gallium nitride and a final layer of gallium nitride. The first surface may be on the final layer of gallium nitride. The conductive layer may connect the plurality of source contacts through vias in the at least one insulating layer. The at least one insulating layer may be heat

conductive and electrically insulating.

A relatively thick layer of a heat conductive metal may be formed over the conductive layer. At least one seed layer may be formed on the conductive layer before the relatively thick layer is formed.

The drain, gate and source connections may be formed by creating then filling vias through the substrate and the epitaxial layers to the drain contact, gate contact and the conductive layer respectively.

Alternatively, the substrate may be removed and the drain, gate and source connections formed by creating then filling vias through the expitaxial layers to the drain contact, gate contact and conductive layer respectively. In this case, a further layer of heat conductive but electrically insulating material may be applied in place of the substrate.

Brief Description of the Drawings

In order that the present invention may be fully understood and readily put into practical effect, there shall now be described by way of non-limitative example only preferred embodiments of the present invention, the description being with reference to the accompanying illustrative drawings.

In the drawings:
Figure 1 is a schematic illustration of a device at a first stage of the fabrication process;
Figure 2 is a schematic illustration of the device at a second stage of the

fabrication process;

Figure 3 is a schematic illustration of the device at a third stage of the fabrication process;

Figure 4 is a schematic illustration of the device at a fourth stage of the fabrication process;

Figure 5 is a schematic illustration of the device at a fifth stage of the fabrication process;

Figure 6 is a schematic illustration of the device at a sixth stage of the fabrication process;

Figure 7 is a schematic illustration of the device at a seventh stage of the fabrication process;

Figure 8 is a schematic illustration of the device at an eighth stage of the fabrication process;

Figure 9 is a schematic illustration of the device at a ninth stage of the fabrication process;

Figure 10 is a schematic illustration of the device at a tenth stage of the fabrication process;

Figure 11 is a schematic illustration of the device at an eleventh stage of the fabrication process;

Figure 12 is a schematic illustration of the device at a twelfth stage of the fabrication process;

Figure 13 is a schematic illustration of the device at a thirteenth stage of the fabrication process;

Figure 14 in a full cross-sectional view along the lines and in the direction of arrows 14 – 14 on Figure 13;

Figure 15 is a schematic illustration of the device at a fourteenth stage of the fabrication process;

Figure 16 a full cross-sectional view along the lines and in the direction of arrows 16 – 16 on Figure 15;

Figure 17 is a schematic illustration of the device at a fifteenth stage of the fabrication process;

Figure 18 is a schematic illustration of the device at a sixteenth stage of the fabrication process;

Figure 19 is a full cross sectional view along the lines and in the direction of arrows 19 – 19 on Figure 18;

Figure 20 is a schematic illustration of the device at a seventeenth stage of the fabrication process;

Figure 21 is a schematic illustration of the device at a final stage of the fabrication process; and

Figure 22 is a schematic illustration of the device at an alternative final stage of the fabrication process.

Detailed Description of the Preferred Embodiments

Figure 1 shows the structure at the commencement of fabrication. A sapphire substrate 1 has a buffer layer 2 above it, and the epitaxial layers 3 are on the buffer layer 2. The epitaxial layers 3 comprise a layer 4 of GaN, a layer 5 of AlGaN, and n+ layer 6 of AlGaN, and a final GaN layer 7.

Source 8 and drain 9 contacts are then formed on the surface of the final GaN layer (Figure 2) there being a source 8 and a drain contact 9 for each transistor. Gate contacts 10 are then formed between each source contact 8 and each drain contact 9 (Figure 3). In this way when each gate 10 is activated current will flow from one source 8 to the two drains 9, one on each side of source

contact 8.

As shown in Figure 4, an electrically insulating layer such as a passivation layer 11 of, for example AlN, is then applied to electrically insulate the contacts 8, 9, 10 while being able to conduct heat. The layer 11 is preferably heat conductive. A resist is applied over passivation layer 11 (Figure 5) and vias 12 formed through passivation layer 11 down to the source contacts 8 and the resist removed. A further layer 13 of an electrically and heat conductive metal is applied over the passivation layer 13, the layer 16 also filling the vias 12. This connects the source contacts 8 (Figure 6). In this way, all contacts 8, 9 and 10 are in the one plane.

As shown in Figure 7, at least one further layer 14 is applied over the conductive metal layer 13 and the passivation layer 11 not covered by the conductive metal layer 13. The further layer 14 is a seed layer.

The seed layer 14 may be a number of layers – for example, three different metal layers. The first seed layer should adhere well to the conductive layer 13 and may be of chromium or titanium. It may be followed by second layer and third layer that may be of tantalum and copper respectively. Other materials may be used for all seed layers. The second seed layer may act as a diffusion barrier, preventing copper or other materials placed on top of it (such as, for example, the third seed layer) from diffusing into the expitaxial layers 3. The third seed layer acts as a seeding layer for subsequent electroplating.

As shown, there are two layers 15, 16 with the layer 15 acting as the diffusion barrier and the other layer 16 being the seeding layer.

The coefficients of thermal expansion of the seed layers may be different from that of GaN which is 3.17. While the thermal expansion coefficients of the contact layers 13 may be different from that of GaN (they are 14.2 and 13.4 respectively), they are relatively thin (a few nanometers) and do not pose serious stress problems to the underlining GaN epitaxial layers. However, plated copper to be added later may be as thick as hundreds of microns and thus may cause severe stress problems. Thus, the seed layers can be used to buffer the stress. This may be by one or more of:

by having sufficient flexibility to absorb the stress,

by having sufficient internal slip characteristics to absorb the stress,

by having sufficient rigidity to withstand the stress, and

by having graded thermal expansion coefficients.

In the case of graded thermal coefficients, that of the first layer preferably less than that of the second layer and that of the second layer is preferably less than that of the third layer and so forth. For example, as shown the first layer 15 may be tantalum with a coefficient of thermal expansion of 6.3, and the second layer 6 may be copper with a coefficient of thermal expansion of 16.5. In this way the coefficients of thermal expansion are graded from the passivation layer 13 and to the outer, copper layer 18. An alternative is to have coefficients of expansion that differ such that at the temperatures concerned, one metal layer expands while another contracts.

If the outer, copper layer 18 was applied directly to the contact layer 13 and passivation layer 11, the differences in their thermal expansion rates may cause cracking, separation, and/or failure. By depositing a plurality of seed layers of

different materials, particularly metals each having a different coefficient of thermal expansion, the stresses of thermal expansion are spread through the seed layers with the resultant lower likelihood of cracking, separation and/or failure. If there are intermediate layer(s), the intermediate layer(s) should have coefficient(s) of expansion between those of layers 15 and 16, and should be graded from that of the first layer 15 to that of the final layer 16. There may be no intermediate layer, or there may be any required or desired number of intermediate layers (one, two, three and so forth).

For patterned plating of a layer 18 of relatively thick metal such as copper that will serve as the new substrate and/or heat sink, a pattern of thick resists 17 is applied to the seed layer 15 by standard photolithography (Figure 8), and the remaining metal 18 is plated between and over the thick resists 17 (Figure 9) to form a single metal support layer 18.

The removal or lift-off of the sapphire substrate 1 then takes place (Figures 10 and 11) in accordance with known techniques such as, for example, that described in Kelly [M.K. Kelly, O. Ambacher, R. Dimitrov, R. Handschuh, and M. Stutzmann, phys. stat. sol. (a) 159, R3 (1997)]. The substrate 1 may also be removed by polishing or wet etching. This exposes the lowermost surface 19 of the GaN layer 4. It is preferred for lift-off of the substrate to take place while the epitaxial layers 3 are intact to improve the quality of removal, and for structural strength. By having the epitaxial layers 3 intact at the time of removal the electrical and mechanical properties of the epitaxial layers 3 are preserved.

After the removal of the original substrate 1, the thickly plated metal 18 is able to act as one or more of: the new mechanical support; and during operation of the

semiconductor device is able to act as one or more of: a heat sink, a heat dissipater, and a connecting layer. As the final GaN layer 7 is relatively thin, the heat generated in active layers 3 is more easily able to be conducted to the thick layer 18. Also, each of the layers 11, 13 and 14 are heat conductive.

The seed layer(s) 14 may be an electrical insulating layer but must be a good thermal conductor e.g. AlN.

The thick layer 18 creates a parasitic capacitance that slows the speed of operation. By increasing the distance between layer 18 and the epitaxial layers 3, the parasitic capacitance is decreased.

A resist layer is applied to the now-exposed surface 19 of the GaN layer 4 and etching takes place to form at least one via 20 through epitaxial layers 13 to the drain contact 9 (Figure 12). Via 20 is then filled (Figure 13) to form a drain connection 21. Figure 14 show a view of the drain connection 20, source contacts 8 and gate contacts 10.

A separate via 22 is formed (Figure 15) through the expitaxial layers 3 to the gate contact 10 and via 22 is filled to form a gate connection 23.

Figure 16 shows a view of the gate connection 23 as well as the drain connection 20, and source contact 8.

Figures 17 and 18 show a similar process for the source connection 8. A via 24 is formed through the expitaxial layers 3 to the source connector layer 13 and the via 24 filled to form the source connection 25.

Figure 19 shows a view of the source connection 25.

Etching then takes place (Figure 20) to form gaps 26 through the epitaxial layers 3, passivation layer 11 and conductive layer 13 until the ends of the thick resists 17 are exposed. The thick resists 17 are then removed for die separation.

This leaves the connections 20, 23 and 25 so the device can be electrically connected. Alternatively, and as shown in Figure 22, the process of Figures 17 and 18 may be avoided with die separation being as described above. Electrical connection for the source contact layer 13 will then be at either or both sides 26.

If desired, the substrate 1 may be left in place and holes drilled by, for examples, lasers to enable the connections 20, 23 and 25 to be formed. Alternatively, and as shown in Figure 21, a further layer 27 of a material that is a heat conductive but electronically insulating (e.g. AlN) may be added in place of substrate 1.

In this way the device HEMT device can be used with the relatively thick metal layer 18 acting as one or more of: a contact, heat sink, heat diffuser, and a physical support for the device. The combined effect of the passivation layer 11, the conductive layer 13, the seed layer 14 and the relatively thick layer 18 is that they are all conductive so they all combine to conduct heat away from the epitaxial layers 3, and for them to combine to be a heat sink.

Whilst there has been described in the foregoing description preferred embodiments of the present invention, it will be understood by those skilled in the technology concerned that many variations or modifications in details of

design or construction may be made without departing from the present invention.

THE CLAIMS

1. A method for fabricating transistors, each transistor comprising a plurality of epitaxial layers on a common substrate, method comprising:
forming a plurality of source contacts on a first surface of the plurality of epitaxial layers;
forming at least one drain contact on the first surface;
forming at least one gate contact on the first surface;
forming at least one layer of insulating material over and between the gate contact, source contacts and the drain contact for insulating the gate contact, source contacts and the drain contact;
forming a conductive layer over and through at least a part of the at least one insulating layer for connecting the source contacts; and
forming at least one heat sink layer over the conductive layer.

2. The method as claimed in claim 1, wherein the transistors are high electron mobility transistors, the plurality of epitaxial layers comprising a layer of gallium nitride, a layer of aluminium gallium nitride, a layer of n+ aluminium gallium nitride and a final layer of gallium nitride, the first surface being on the final layer of gallium nitride; the at least one layer of insulating material being electrically insulating but heat conductive; the conductive layer connecting the plurality of source contacts through vias in the at least one insulating layer.

3. The method as claimed in claim 1 or claim 2, wherein a relatively thick layer of conductive metal is formed over the conductive layer.

4. The method as claimed in claim 3, wherein a seed layer is formed on the conductive layer before the relatively thick layer is formed.

5. The method as claimed in claim 4 wherein the seed layer comprises a plurality of seed layers, wherein a first of the plurality of seed layers is applied to the conductive layer, the first seed layer being of a material that has a first co-efficient of thermal expansion; and a second seed layer is formed on the first seed layer, the second seed layer being of a material that has a second co-efficient of thermal expansion, the second co-efficient of thermal expansion being greater than the first co-efficient of thermal expansion.

6. The method as claimed in claim 5, wherein one of the first seed layer and the second seed layer is a diffusion barrier for providing a barrier to diffusion of a layer applied to it from diffusing into the expitaxial layers.

7. A method as claimed in any one of claims 3 to 6, wherein the relatively thick layer is for at least one selected from the group consisting of: a structural support, a heat sink, a heat dissipater, and as a connector.

8. The method as claimed in any one of claims 1 to 7, wherein a source connection is formed by creating then filling at least one via through the common substrate and the plurality of epitaxial layers to the conductive layer.

9. The method is claimed in anyone of claims 1 to 8, wherein a drain connection is formed by creating then filing at least one via through the common substrate and the plurality of epitaxial layers to the at least one drain contact.

10. The method as claimed in any one of claims 1 to 9, wherein a gate connection is formed by creating then filling at least one via through the common substrate and the plurality of epitaxial layers to the at least one gate

contact.

11. The method as claimed in any one of claims 3 to 7 further comprising removing the substrate after the relatively thick layer is formed; and forming a further layer of electrically insulating and heat conductive material in place of the substrate.

12. The method as claimed in claim 11, wherein a source connection is formed by forming then filling at least one via through the plurality of epitaxial layers to the conductive layer.

13. The method is claimed in anyone of claim 11 or claim 12, wherein a drain connection is formed by creating then filing at least one via through the plurality of epitaxial layers to the at least one drain contact.

14. The method as claimed in any one of claims 11 to 13, wherein a gate connection is formed by creating then filling at least one via through the plurality of epitaxial layers to the at least one gate contact.

15. The method as claimed in any one of claims 3 to 14, wherein patterned plating is performed before the relatively thick layer is formed.

16. Apparatus comprising transistors, each comprising:

(a) a plurality of epitaxial layers having a first surface;

(b) a plurality of source contacts, at least one drain contact and at least one gate contact, all on the first surface;

(c) at least one insulating layer over and between the source contacts, the at least one drain contact and the at least one gate contact for insulating the

gate contact, source contact and the drain contact;

(d) a conductive layer over and through at least a part of the at least one insulating layer for connecting the source contacts; and

(f) at least one heat sink layer over the conductive layer.

17. The apparatus as claimed in claim 16, wherein the at least one heat sink layer is over a reminder of the at least one insulating layer not covered by the conductive layer.

18. The apparatus as claimed in claim 17, wherein the at least one insulating layer is electrically insulating and heat conductive.

19. The apparatus as claimed in any one of claims 16 to 18, wherein the plurality of epitaxial layers comprises a layer of gallium nitride, layer of aluminum gallium nitride, a layer of n+ aluminum gallium nitride and a final layer of gallium nitride, the first surface being on the final layer of gallium nitride.

20. The apparatus as claimed in any one of claims 16 to 19, wherein the conductive layer connects the plurality of source contacts through vias in the at least one insulating layer.

21. The apparatus as claimed in any one of claims 16 to 20 further comprising a relatively thick layer of conductive metal over the conductive layer.

22. The apparatus as claimed in claim 21 further comprising at least one seed layer between the conductive layer and the relatively thick layer.

23. The apparatus as claimed in claim 22, wherein the seed layer comprises a plurality of seed layers, wherein a first of the plurality of seed layers is on the conductive layer, the first seed layer being of a material that has a first co-efficient of thermal expansion; and a second seed layer is on the first seed layer, the second seed layer being of a material that has a second co-efficient of thermal expansion, the second co-efficient of thermal expansion being greater than the first co-efficient of thermal expansion.

24. The apparatus as claimed in claim 23, wherein one of the first seed layer and the second seed layer is a diffusion barrier for providing a barrier to diffusion of a layer applied to it from diffusing into the expitaxial layers.

25. The apparatus as claimed in any one of claims 21 to 24, wherein the relatively thick layer is for at least one selected from the group consisting of: a structural support, a heat sink, a heat dissipater, and a connector.

26. The apparatus as claimed in any one of claims 16 to 25 further comprising a source connection through the common substrate and the plurality of epitaxial layers to the conductive layer.

27. The apparatus as claimed in any one of claims 16 to 26 further comprising a drain connection through the common substrate and the plurality of epitaxial layers to the at least one drain contact.

28. The apparatus as claimed in any one of claims 16 to 27 further comprising a gate connection through the common substrate and the plurality of epitaxial layers to the at least one gate contact.

29. The apparatus as claimed in any one of claims 16 to 25 wherein the substrate is removed after the relatively thick layer is formed.

30. The apparatus as claimed in claim 29 further comprising a source connection through the plurality of epitaxial layers to the conductive layer.

31. The apparatus as claimed in claim 29 or claim 30 further comprising a drain connection through the plurality of epitaxial layers to the at least one source contact.

32. The apparatus as claimed in any one of claims 29 to 31 further comprising a gate connection through and the plurality of epitaxial layers to the at least one gate contact.

33. The apparatus as claimed in any one of claims 22 to 25, wherein the at least one heat sink layer comprises the relatively thick layer, the at least one seed layer, the conductive layer and the pat least one insulating layer.

34. The apparatus as claimed in any one of claims 16 to 33, wherein the transistors are high electron mobility transistors.

35. The apparatus as claimed in any one of claims 29 to 32 further comprising a layer of electrically insulating and heat conductive material in place of the substrate.

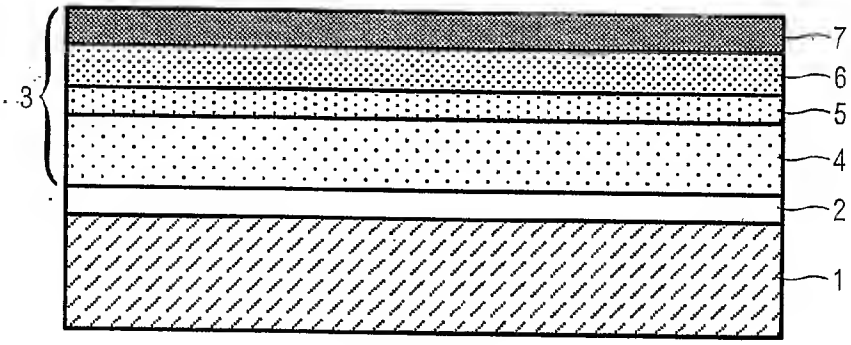


FIG. 1

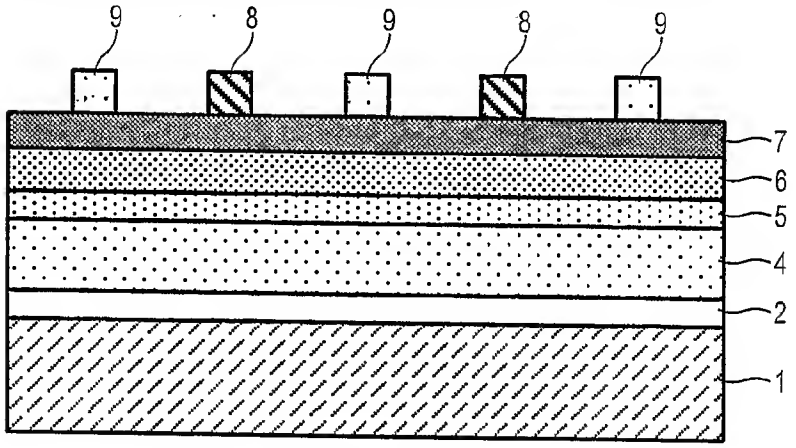


FIG. 2

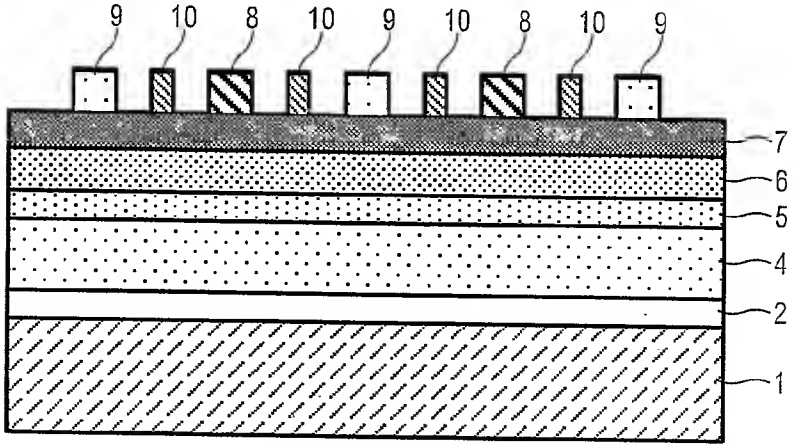


FIG. 3

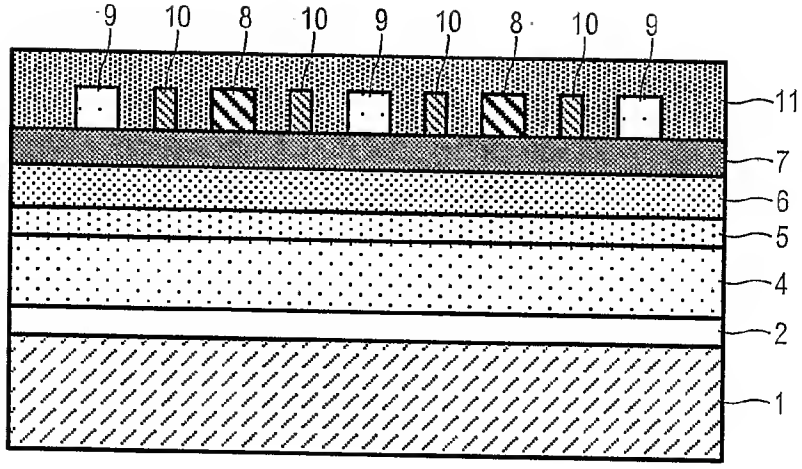


FIG. 4

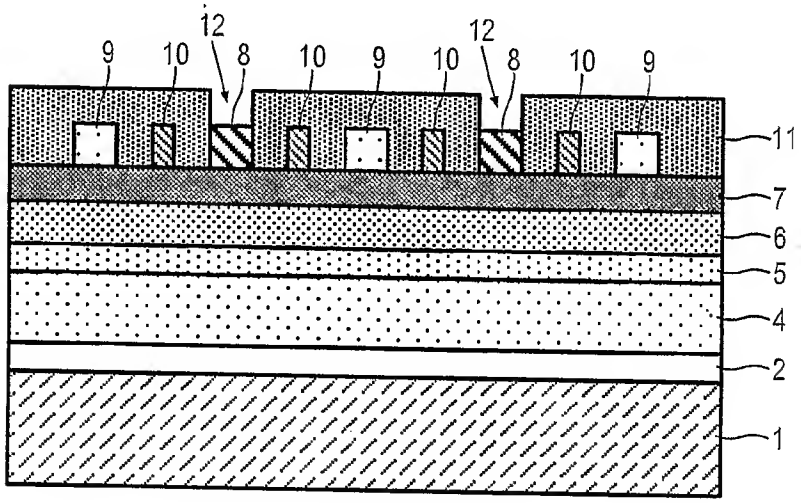


FIG. 5

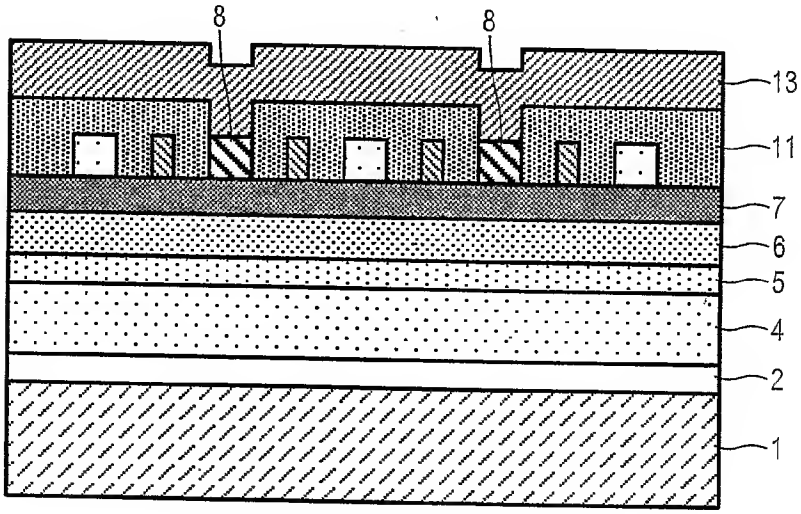


FIG. 6

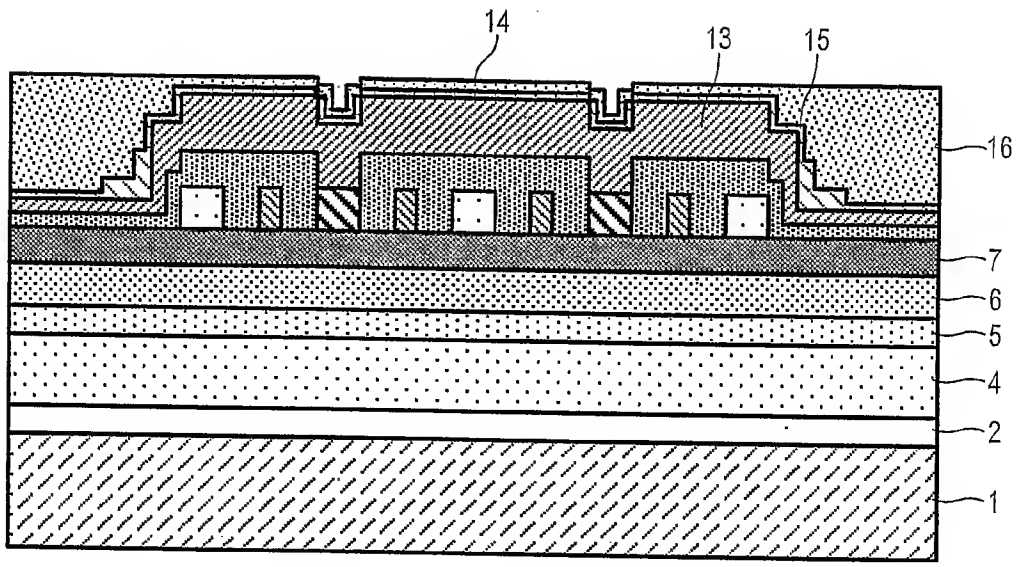


FIG. 7

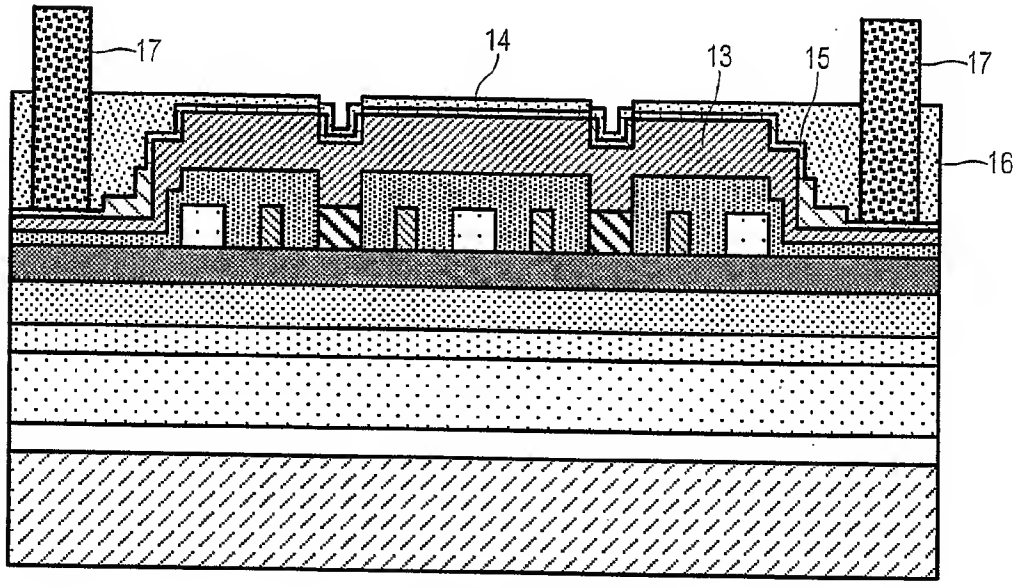


FIG. 8

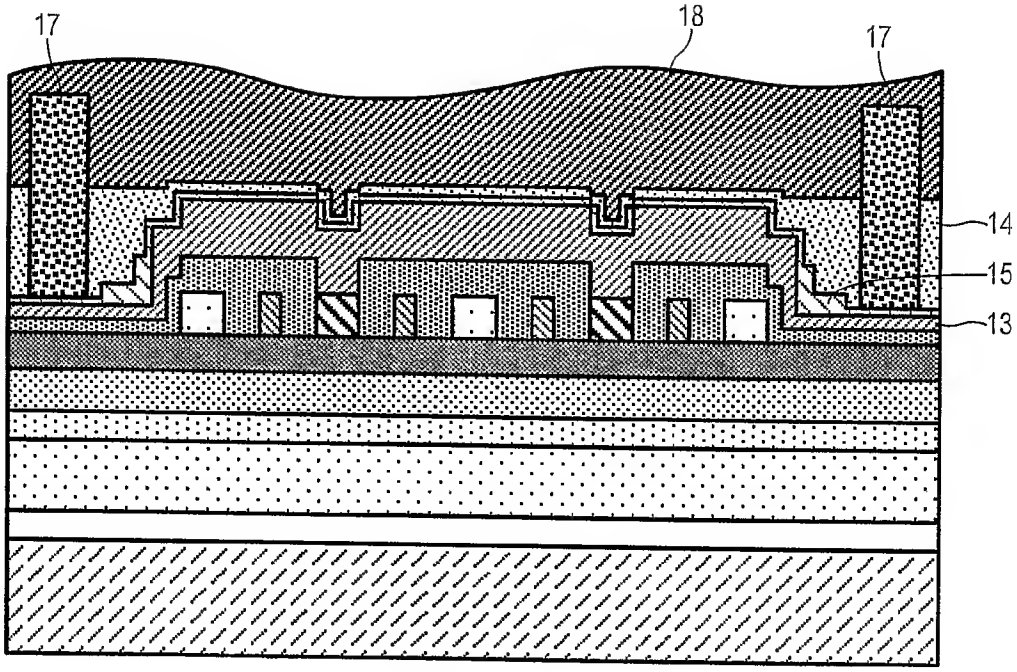


FIG. 9

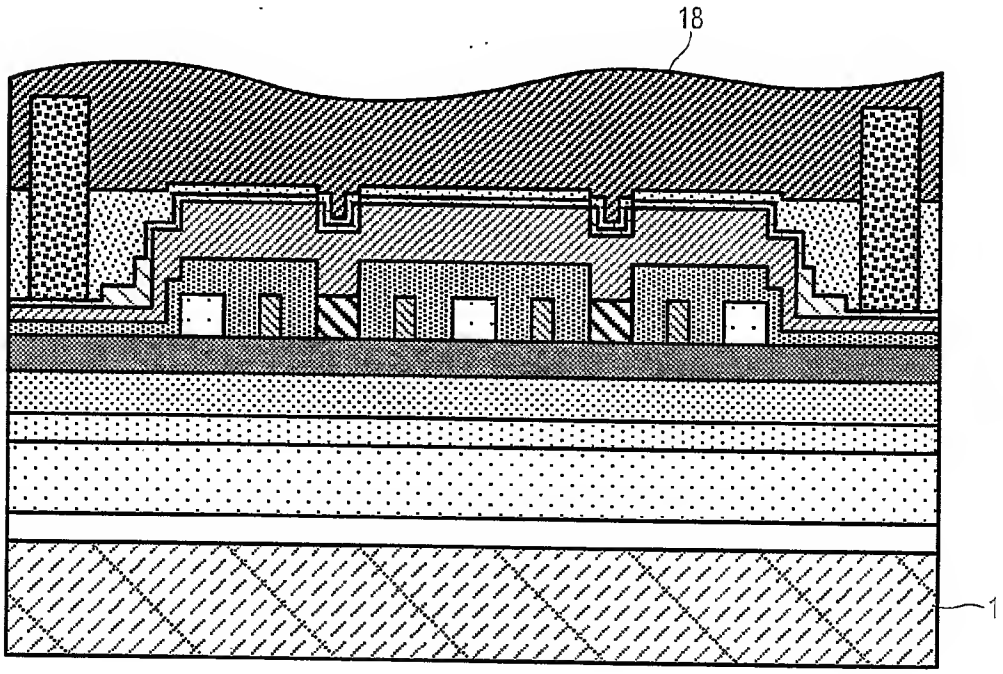


FIG. 10

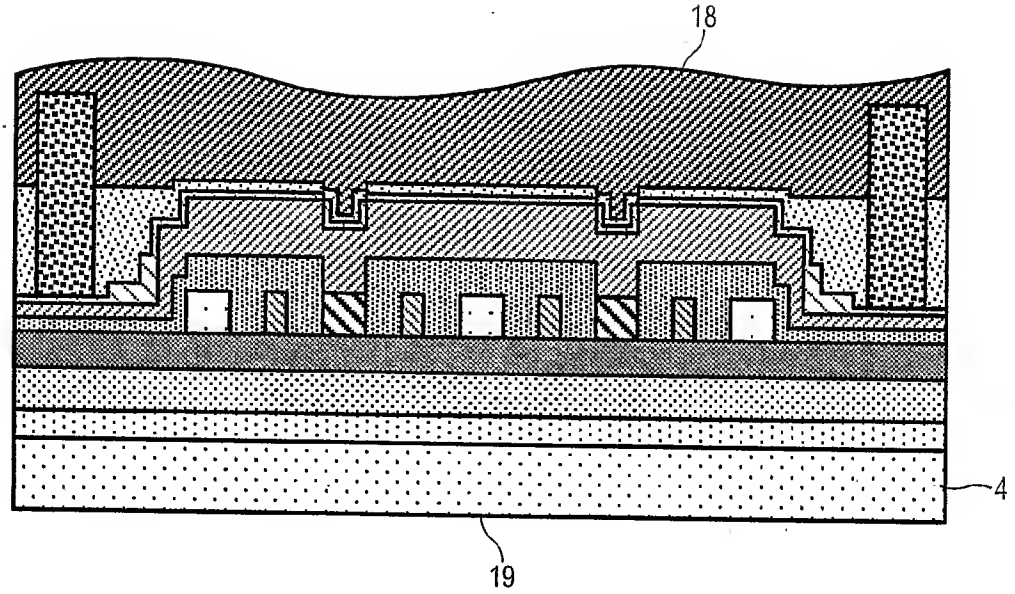


FIG. 11

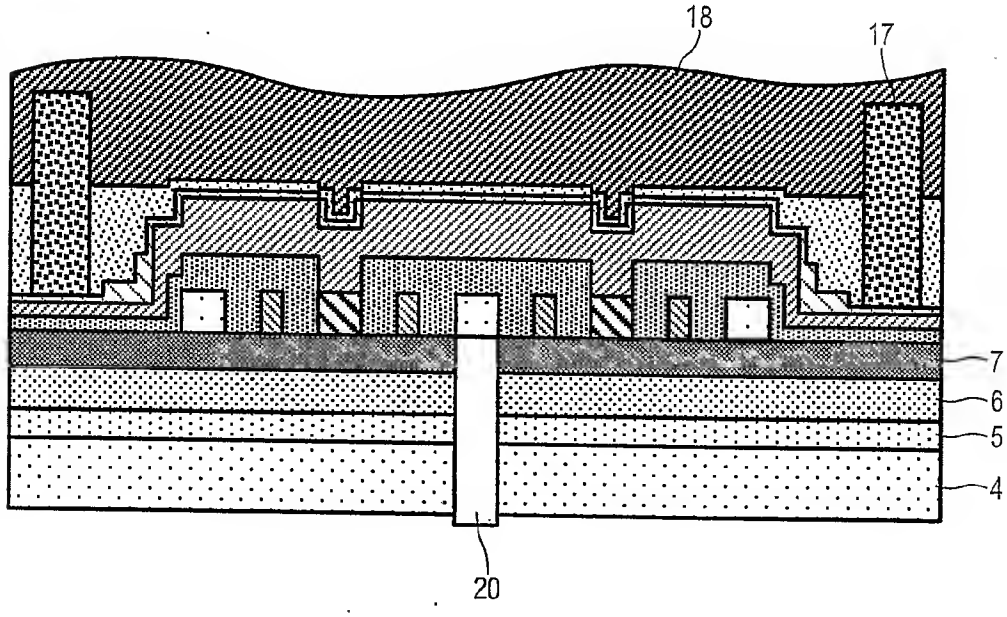


FIG. 12

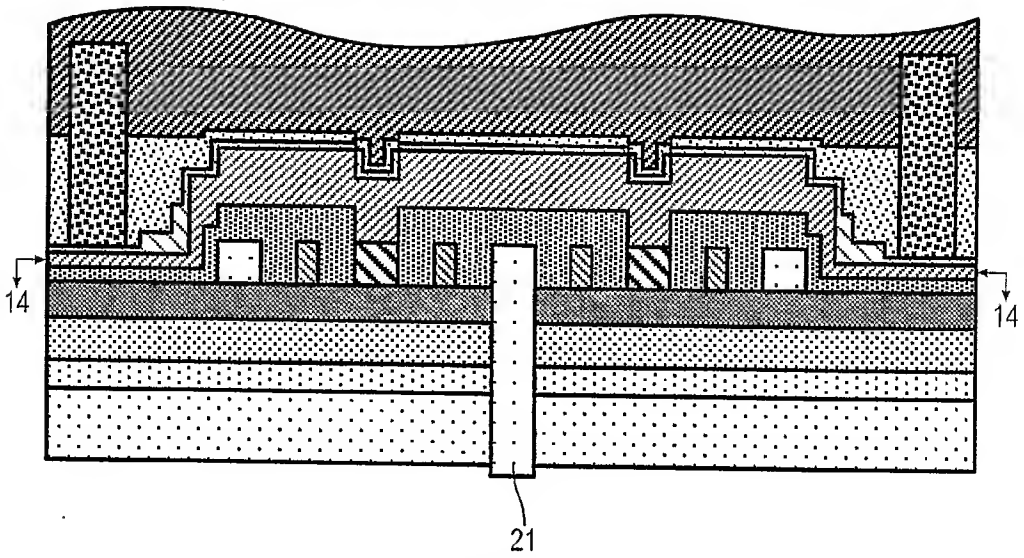


FIG. 13

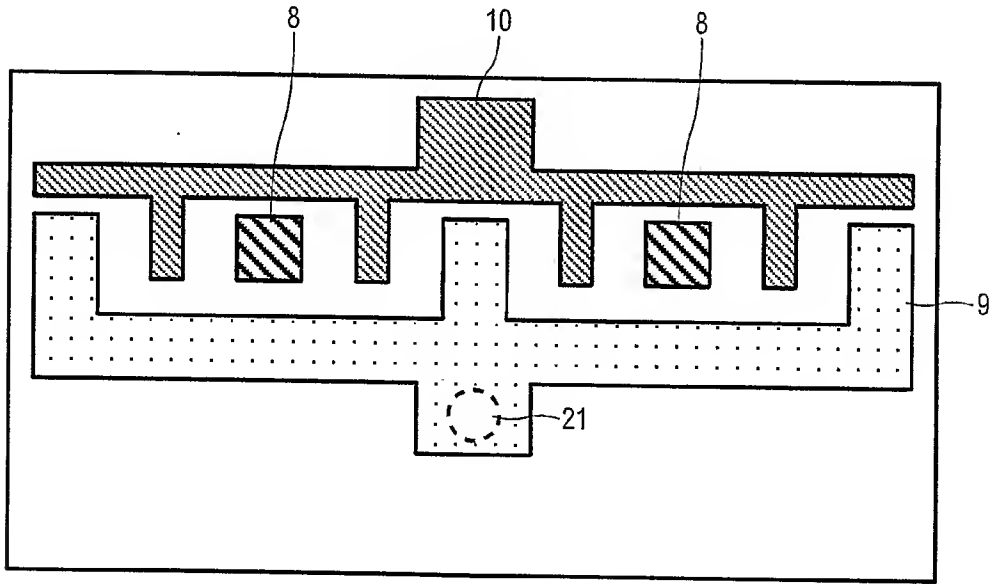


FIG. 14

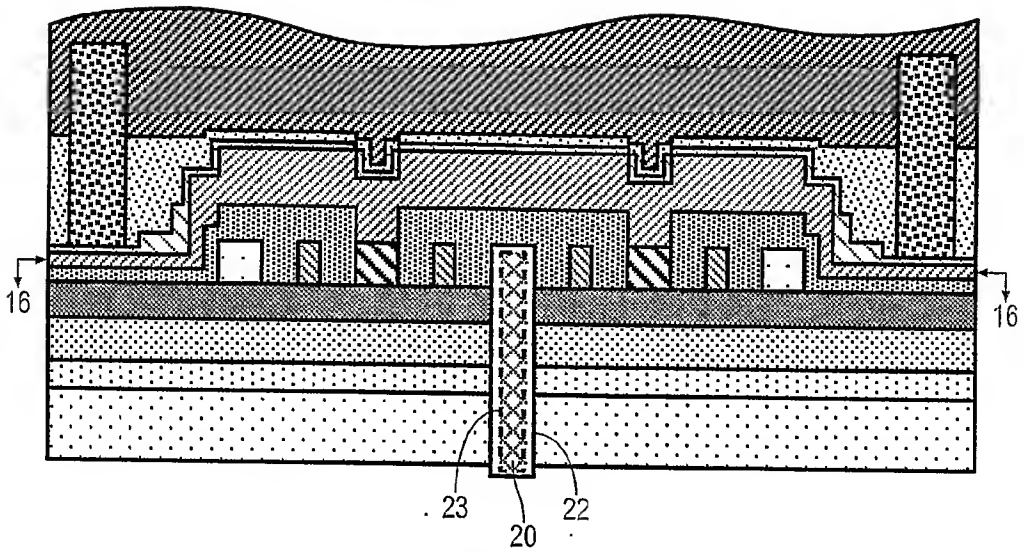


FIG. 15

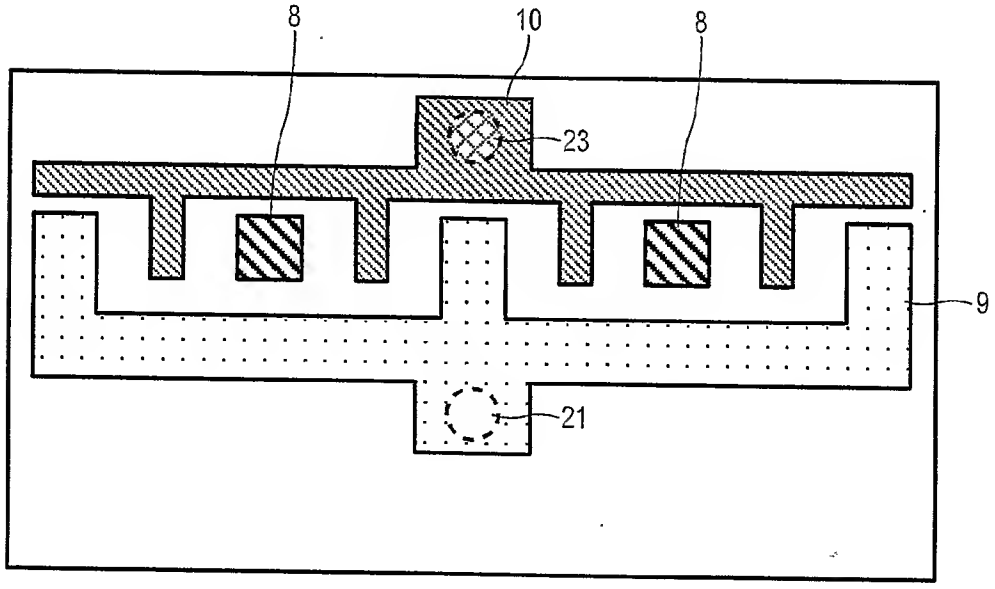


FIG. 16

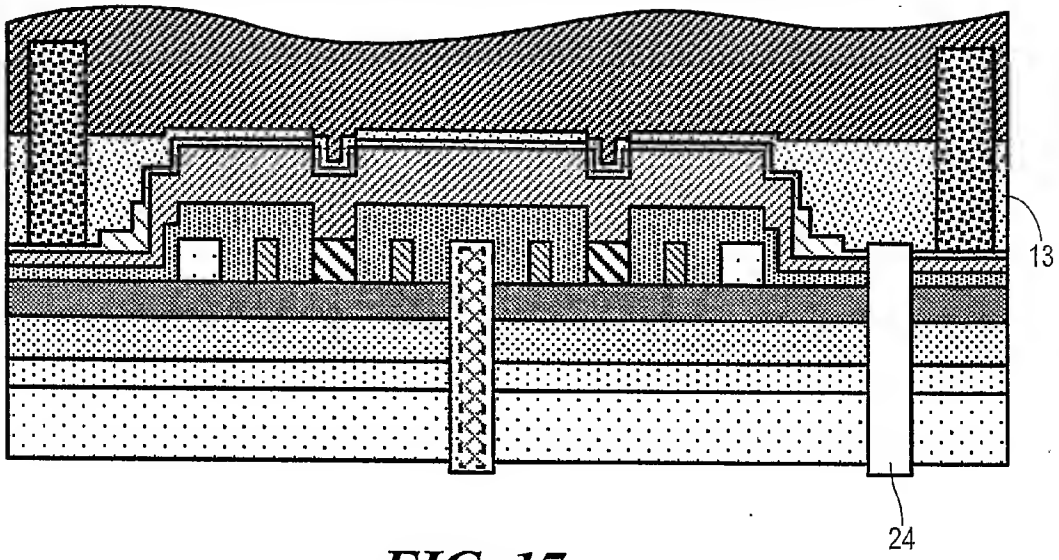


FIG. 17

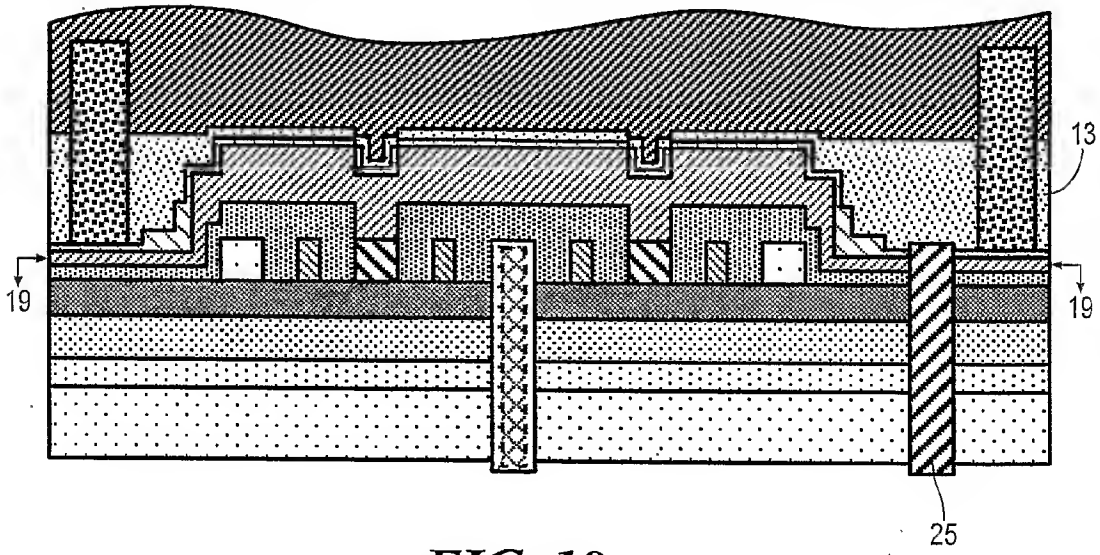


FIG. 18

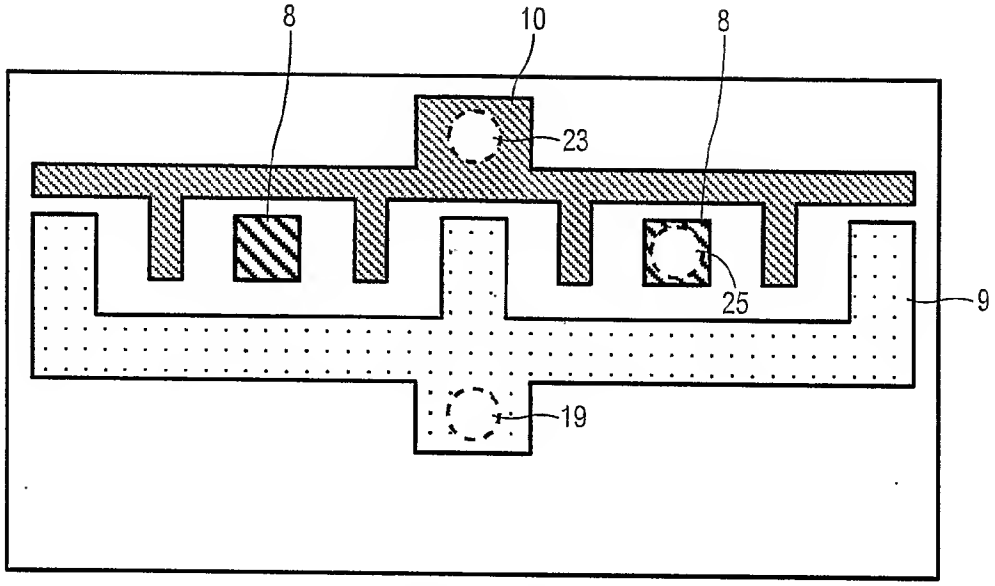


FIG. 19

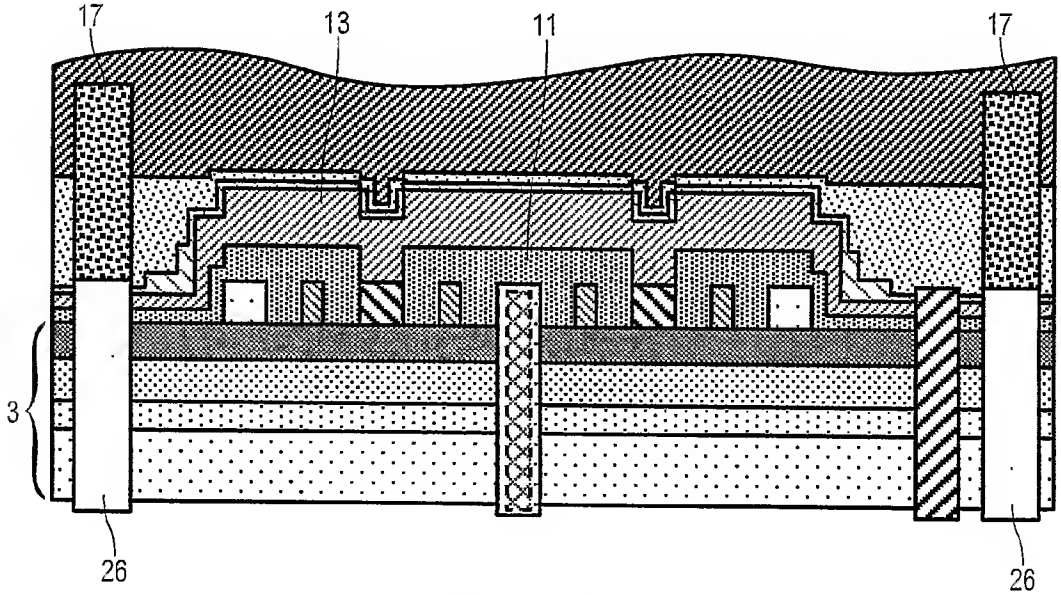


FIG. 20

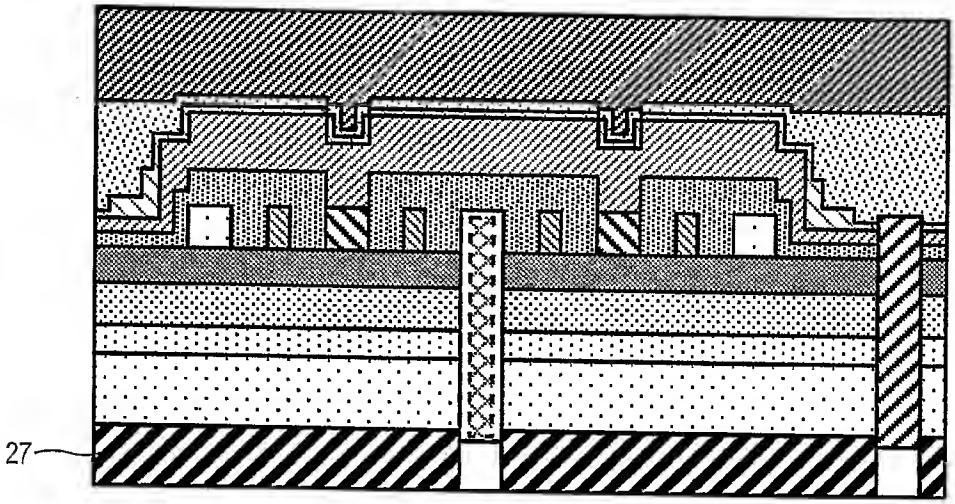


FIG. 21

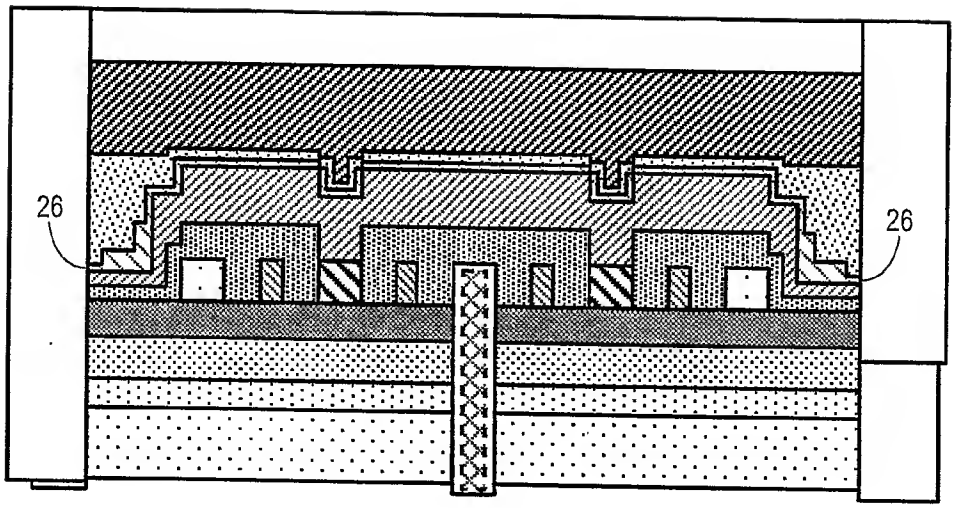


FIG. 22

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2006/000255

A. CLASSIFICATION OF SUBJECT MATTER

Int. Cl.

H01L 27/082 (2006.01) ***H01L 21/02*** (2006.01) ***H01L 29/737*** (2006.01)

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)
DWPI and keywords: transistors, HEMT, HFET, HBT, bipolar, high electron mobility, hetero-junction, epitaxial, GaN, gallium nitride, aluminium gallium nitride, heat, sink, dissipate, source, drain, gate, connection, contact, insulator, conductive, layer, surface, heat, material, and other similar terms.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2005/0127397 A1 (BORGES ET AL) 16 June 2005 See figure 9, paragraphs 55-70	1-3, 7-14, 16-21, 25-35
Y	US 2002/0117681 A1 (WEEKS ET AL) 29 August 2002 See figures 7 and 8, paragraphs 59-61	1-3, 7-14, 16-21, 25-35
Y	US 5192987 A (KHAN ET AL) 9 March 1993 See figures 1, 3, 5, 6, and columns 1-4	1-3, 7-14, 16-21, 25-35

[X] Further documents are listed in the continuation of Box C [X] See patent family annex

* Special categories of cited documents:

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier application or patent but published on or after the international filing date

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
25 October 2006	6 NOV 2006
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200, WODEN ACT 2606, AUSTRALIA E-mail address: pct@ipaustralia.gov.au Facsimile No. (02) 6285 3929	Authorized officer **Lynn Bloomfield** Telephone No : (02) 6283 2851

INTERNATIONAL SEARCH REPORT

International application No.
PCT/SG2006/000255

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 2004/0130037 A1 (MISHRA ET AL) 8 July 2004 See figures 3, 4, 9-11 and paragraphs 46-52, 60-65	1-3, 7-14, 16-21, 25-35
A	US 2005/0164482 A1 (SAXLER) 28 July 2005 See entire document	
A	US 4107720 A (PUCEL ET AL) 15 August 1978 See entire document	
	Claims 1-3, 7-14, 16-21, 25-35 are not inventive when document US 2005/0127397 is combined with either US 2002/0117681, US 5192987, or US 2004/0130037.	

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/SG2006/000255

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report		Patent Family Member					
US	4107720	CA	1027257	DE	2548483	FR	2290041
		GB	1482337	JP	51067076	US	4016643
US	2002117681	EP	1378012	US	6611002	US	2004130002
		WO	02069410	WO	2005022639		
US	5192987	US	5296395				
US	2004130037	AU	2003300000	CA	2511005	CN	1757119
		EP	1579509	US	6825559	US	2005006669
		US	2005067716	WO	2004061973		
US	2005164482	CA	2554003	EP	1706895	US	7033912
		US	2006138455	WO	2005074013		
US	2005127397	AU	2002306569	EP	1386354	US	6956250
		US	2002117695	WO	02069373		

Due to data integration issues this family listing may not include 10 digit Australian applications filed since May 2001.

END OF ANNEX